

# **NP110N055PUK**

# MOS FIELD EFFECT TRANSISTOR

R07DS0591EJ0100 Rev.1.00 Dec 12, 2011

#### **Description**

The NP110N055PUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### **Features**

• Super low on-state resistance

 $R_{DS(on)} = 1.75 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 55 \text{ A})$ 

- Low  $C_{iss}$ :  $C_{iss} = 10700 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

#### **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP110N055PUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP110N055PUK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

## **Absolute Maximum Ratings** $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	55	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	± <b>20</b>	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±110	A
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	±440	A
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	348	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to 175	°C
Repetitive Avalanche Current *2	I <sub>AR</sub>	66	А
Repetitive Avalanche Energy *2	E <sub>AR</sub>	435	mJ

Notes: \*1 T<sub>C</sub> = 25°C,  $P_W \le 10~\mu s$ , Duty Cycle  $\le 1\%$ 

#### **Thermal Resistance**

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.43	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	83.3	°C/W

<sup>\*2</sup> R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V

# **Electrical Characteristics** $(T_A = 25^{\circ}C)$

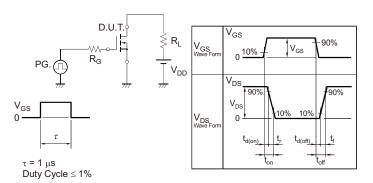
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1	μΑ	V <sub>DS</sub> = 55 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Forward Transfer Admittance *1	y <sub>fs</sub>	60	120	_	S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 55 A
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>	_	1.45	1.75	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 55 A
Input Capacitance	C <sub>iss</sub>	_	10700	16050	pF	V <sub>DS</sub> = 25 V
Output Capacitance	Coss	_	1200	1800	pF	V <sub>GS</sub> = 0 V
Reverse Transfer Capacitance	C <sub>rss</sub>	_	380	690	pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>	_	38	90	ns	V <sub>DD</sub> = 28 V, I <sub>D</sub> = 55 A
Rise Time	t <sub>r</sub>	_	19	50	ns	V <sub>GS</sub> = 10 V
Turn-off Delay Time	t <sub>d(off)</sub>	_	140	280	ns	$R_G = 0 \Omega$
Fall Time	t <sub>f</sub>	_	14	40	ns	
Total Gate Charge	$Q_G$	_	196	294	nC	V <sub>DD</sub> = 44 V
Gate to Source Charge	$Q_{GS}$	_	51	_	nC	V <sub>GS</sub> = 10 V
Gate to Drain Charge	$Q_{GD}$	_	45	_	nC	I <sub>D</sub> = 110 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$	_	0.9	1.5	V	I <sub>F</sub> = 110 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	_	83	_	ns	I <sub>F</sub> = 110 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>	_	145	_	nC	di/dt = 100 A/μs

Note: \*1 Pulsed test

#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DS}$ $V_{DS}$ $V_{DS}$ $V_{DS}$

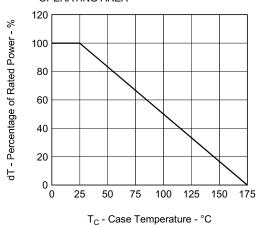
#### TEST CIRCUIT 2 SWITCHING TIME



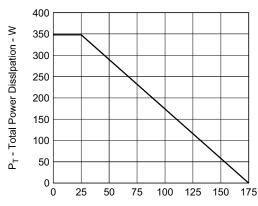
#### **TEST CIRCUIT 3 GATE CHARGE**

## **Typical Characteristics** $(T_A = 25^{\circ}C)$

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

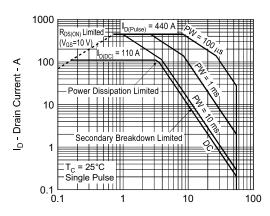


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



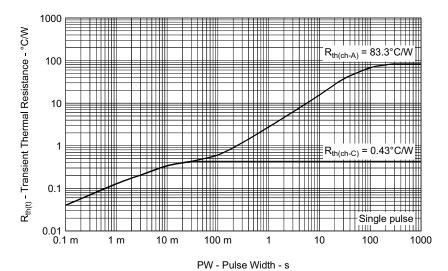
T<sub>C</sub> - Case Temperature - °C

#### FORWARD BIAS SAFE OPERATING AREA



V<sub>DS</sub> - Drain to Source Voltage - V

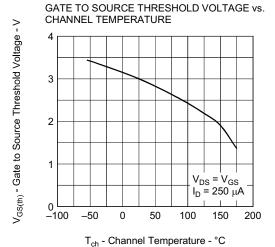
## TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



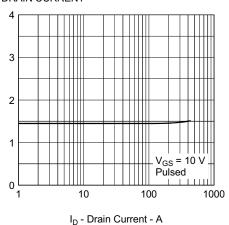
#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE 500 400 I<sub>D</sub> - Drain Current - A 300 200 100 $V_{GS} = 10 \text{ V}$ Pulsed 0 0 0.2 0.4 0.6 8.0



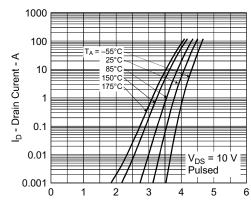
V<sub>DS</sub> - Drain to Source Voltage - V



DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT** 

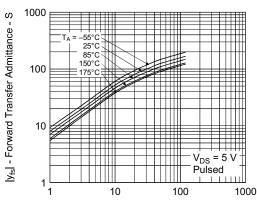


#### FORWARD TRANSFER CHARACTERISTICS



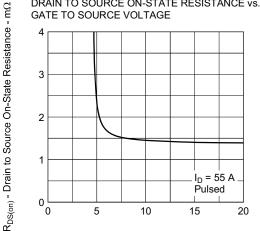
V<sub>GS</sub> - Gate to Source Voltage - V

#### FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I<sub>D</sub> - Drain Current - A

#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

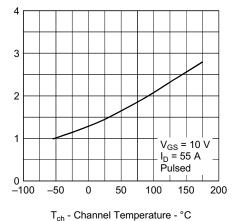


V<sub>GS</sub> - Gate to Source Voltage - V

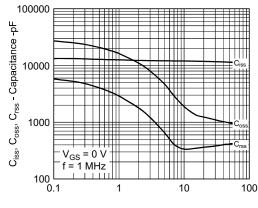
 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 



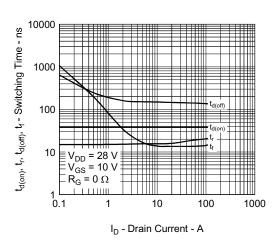


# CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

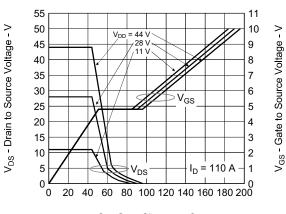


V<sub>DS</sub> - Drain to Source Voltage - V

#### SWITCHING CHARACTERISTICS

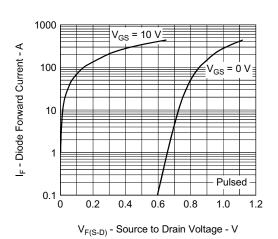


#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS

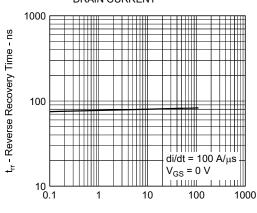


Q<sub>G</sub>- Gate Charge - nC

#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



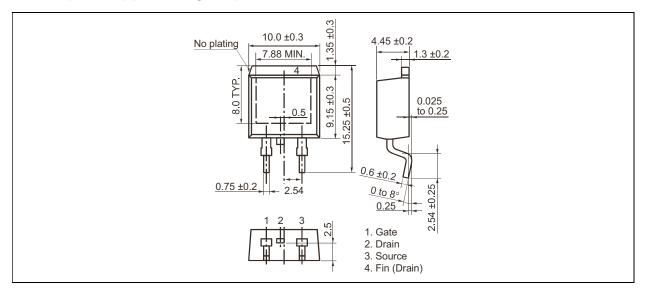
# REVERSE RECOVERY TIME vs. DRAIN CURRENT



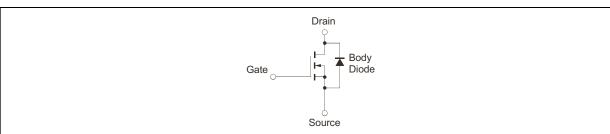
I<sub>F</sub> - Drain Current - A

## Package Drawing (Unit: mm)

## TO-263 (MP-25ZP) (Mass: 1.5 g TYP.)



# **Equivalent Circuit**



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

## NP110N055PUK Data Sheet

		Description			
Rev	v. Date	Page	Summary		
1.00	Dec 12, 2011	_	First Edition Issued		

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