

March 2013

FQP13N50 / FQPF13N50

N-Channel QFET MOSFET

500 V, 12.5 A, 430 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 12.5 A, 500 V, $R_{DS(on)}$ = 430 m Ω (Max) @ V_{GS} = 10 V, I_D = 6.25 A
- Low Gate Charge (Typ. 45 nC)
- Low Crss (Typ. 25 pF)
- · 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter		FQP13N50	FQPF13N50	Unit
V_{DSS}	Drain-Source Voltage		5	V	
I _D	Drain Current - Continuous (T _C = 25°C)		12.5	12.5 *	Α
	- Continuous (T _C = 100°C)		7.9	7.9 *	Α
I_{DM}	Drain Current - Pulsed	(Note 1)	50	50 *	Α
V _{GSS}	Gate-Source Voltage		± 30		V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	810		mJ
I _{AR}	Avalanche Current	(Note 1)	12.5		Α
E _{AR}	Repetitive Avalanche Energy (N		17		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_{D}	Power Dissipation (T _C = 25°C)		170	56	W
	- Derate above 25°C		1.35	0.45	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

^{*} Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FQP13N50	FQPF13N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.74	2.23	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5		°C/W

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$, Referenced to 25°C		0.48		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 400 V, T _C = 125°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10 V, I _D =6.25 A		0.33	0.43	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 50 \text{ V}, I_D = 6.25 \text{ A}$ (Note 4)		10		S
C _{oss} C _{rss}	Output Capacitance Reverse Transfer Capacitance	f = 1.0 MHz		245 25	320 35	pF pF
C _{rss}	Reverse Transfer Capacitance			25	35	pF
Switch	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 13.4 A,		40	90	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		140	290	ns
t _{d(off)}	Turn-Off Delay Time			100	210	ns
t _f	Turn-Off Fall Time	(Note 4, 5)		85	180	ns
Q_g	Total Gate Charge	V _{DS} = 400 V, I _D = 13.4 A,		45	60	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		11		nC
Q _{gd}	Gate-Drain Charge	(Note 4, 5)		22		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
	Maximum Continuous Drain-Source Diode Forward Current				12.5	Α
I_S	Maximum Pulsed Drain-Source Diode Forward Current				50	Α
	Maximum Pulsed Drain-Source Diode F	orward Current			50	_ A
I _{SM}	Maximum Pulsed Drain-Source Diode F Drain-Source Diode Forward Voltage	Forward Current $V_{GS} = 0 \text{ V, I}_{S} = 12.5 \text{ A}$			1.4	V
I _S I _{SM} V _{SD}						

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 9.3mH, $l_{AS} = 12.5A, V_{DD} = 50V, R_G = 25 \,\Omega,$ Starting $T_J = 25^{\circ}C$ 3. $l_{SD} \leq 13.4A,$ di/dt $\leq 200\text{A}/\mu\text{s},$ $V_{DD} \leq BV_{DSS},$ Starting $T_J = 25^{\circ}C$ 4. Pulse Test : Pulse width $\leq 300\mu\text{s},$ Duty cycle $\leq 2\%$ 5. Essentially independent of operating temperature

Typical Characteristics

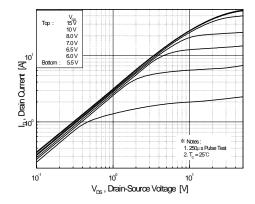


Figure 1. On-Region Characteristics

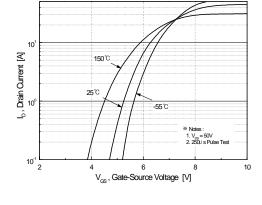


Figure 2. Transfer Characteristics

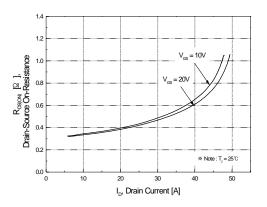


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

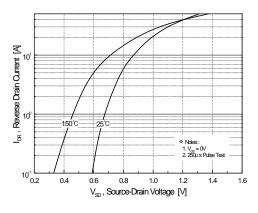


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

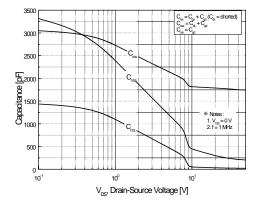


Figure 5. Capacitance Characteristics

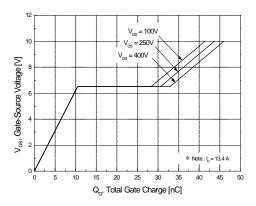


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

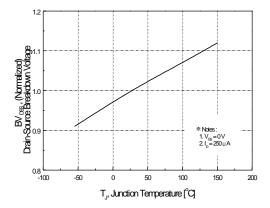


Figure 7. Breakdown Voltage Variation vs. Temperature

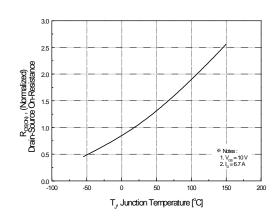


Figure 8. On-Resistance Variation vs. Temperature

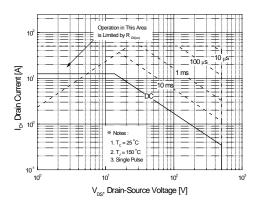


Figure 9-1. Maximum Safe Operating Area for FQP13N50

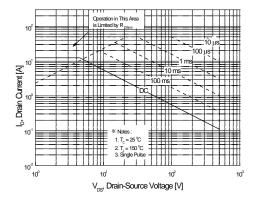


Figure 9-2. Maximum Safe Operating Area for FQPF13N50

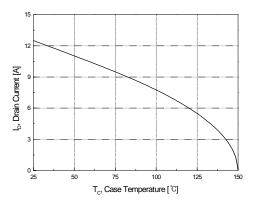


Figure 10. Maximum Drain Current vs. Case Temperature

Typical Characteristics (Continued)

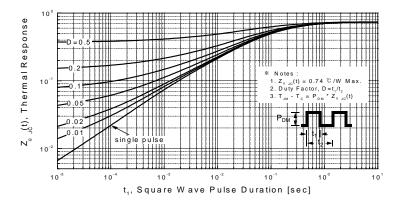


Figure 11-1. Transient Thermal Response Curve for FQP13N50

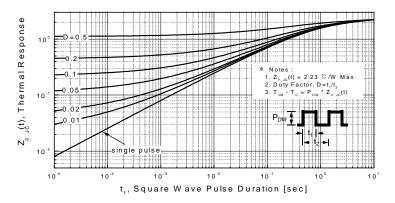
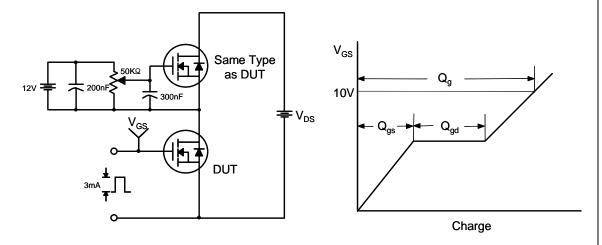
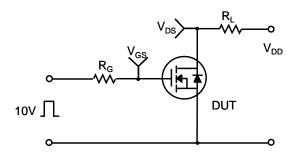


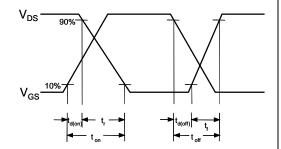
Figure 11. Transient Thermal Response Curve for FQPF13N50

Gate Charge Test Circuit & Waveform

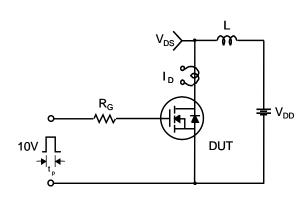


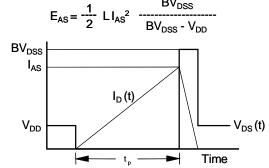
Resistive Switching Test Circuit & Waveforms



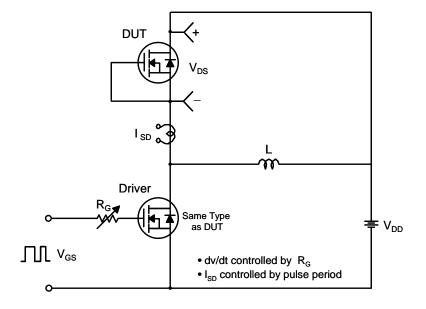


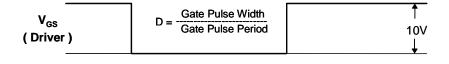
Unclamped Inductive Switching Test Circuit & Waveforms

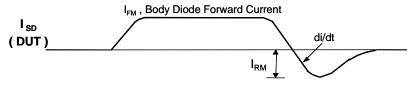




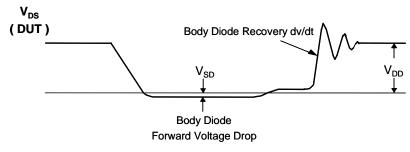
Peak Diode Recovery dv/dt Test Circuit & Waveforms

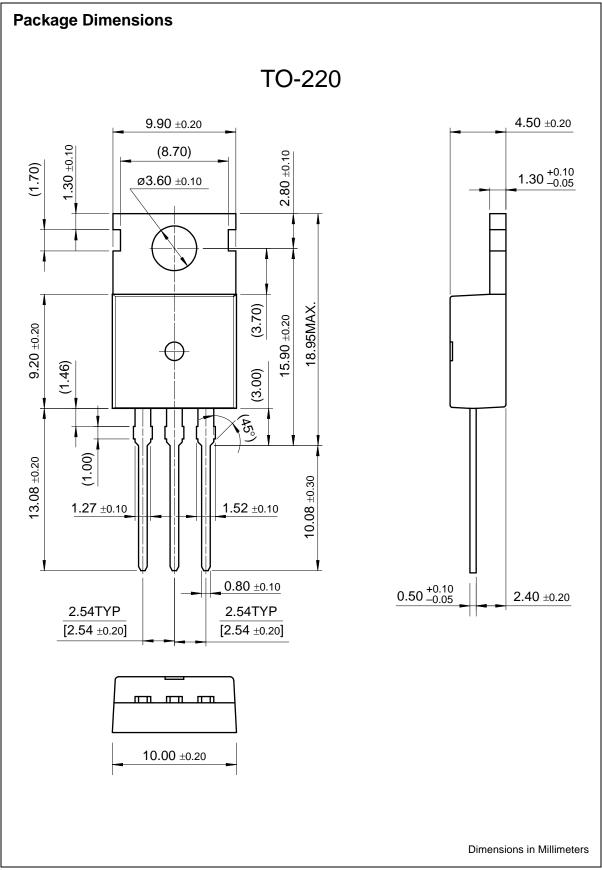


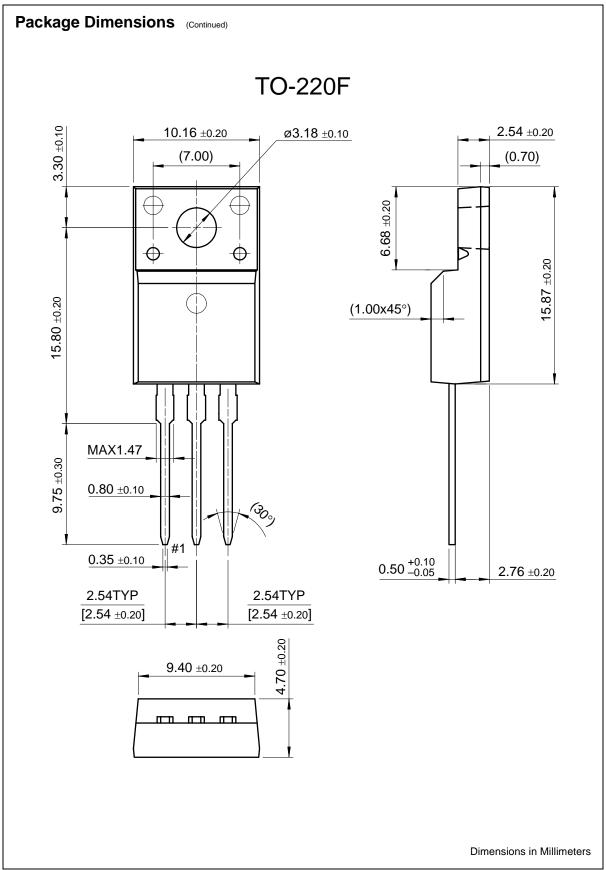




Body Diode Reverse Current











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