

Si4410DY*

Single N-Channel Logic Level PowerTrench MOSFET

General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

This device is well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Applications

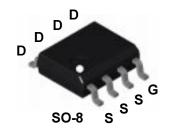
- · Battery switch
- · Load switch
- Motor controls

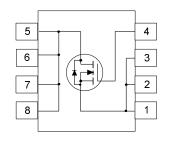
Features

• 10 A, 30 V.
$$R_{DS(ON)} = 0.0135 \Omega @ V_{GS} = 10 V$$

 $R_{DS(ON)} = 0.020 \Omega @ V_{GS} = 4.5 V$

- · Low gate charge.
- · Fast switching speed.
- High performance trench technology for extremely low $R_{_{\mathrm{DS(ON)}}}.$
- · High power and current handling capability.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units V	
V _{DSS}	Drain-Source Voltage	30		
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Drain Current - Continuous	(Note 1a)	10	A
	- Pulsed		50	
P _D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T _J , T _{STG}	Operating and Storage Junction Temperatur	-55 to +150	∘C	

Thermal Characteristics

R _{eJA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	∘C/W
R _{eJC}	Thermal Resistance, Junction-to-Case	(Note 1)	25	∘C/W

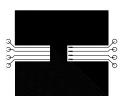
Package Outlines and Ordering Information

Device Marking		Device	Reel Size	Tape Width	Quantity
4410		SI4410DY	13"	12mm	2500 units

^{*} Die and manufacturing source subject to change without prior notification.

Symbol	Parameter	Test Conditions		Тур	Max	Units
Off Char	acteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	30			٧
$\frac{\Delta BVDSS}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		21		mV/∘C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 30 V, V _{GS} = 0 V V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55∘C			1 25	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	1			V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		-4.5		mV/∘C
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}, T_J = 125 ^{\circ}\text{C}$ $V_{GS} = 4.5 \text{ V}, I_D = 8 \text{ A}$		0.011 0.018 0.017	0.0135 0.032 0.020	Ω
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	20			Α
g FS	Forward Transconductance	V _{DS} = 10 V, I _D = 10 A		27		S
Dynamic	Characteristics		ļ			
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V,		1350		pF
Coss	Output Capacitance	f = 1.0 MHz		340		pF
C _{rss}	Reverse Transfer Capacitance			125		pF
Switchir	ng Characteristics (Note 2)				
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 25 \text{ V}, I_D = 1 \text{ A}, R_L = 25 \Omega$			30	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V, } R_{GEN} = 6 \Omega$			20	ns
t _{d (off)}	Turn-Off Delay Time				100	ns
t _f	Turn-Off Fall Time				80	ns
t _{rr}	Drain-Source Reverse Recovery Time	$I_F = 2.3A$, di/dt = $100A/\mu s$			80	nS
Q_g	Total Gate Charge	V _{DS} = 15 V, I _D = 10 A,		22	60	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		5		nC
Q_{gd}	Gate-Drain Charge			4		nC
Drain-So	ource Diode Characteris	tics and Maximum Ratings				
Is		ontinuous Drain-Source Diode Forward Current			2.3	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.3 A (Note 2)		0.7	1.1	V

^{1:} R_{0,J} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50° C/W when mounted on a 1 in² pad of 2 oz. copper.



b) 105° C/W when mounted on a 0.04 in² pad of 2 oz. copper.

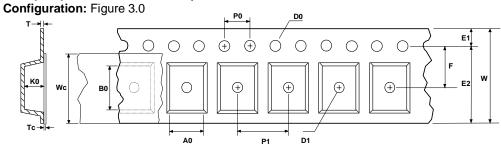


Scale 1 : 1 on letter size paper 2: Pulse Test: Pulse Width \leq 300 $\mu s, \, Duty \, Cycle \leq$ 2.0%

SOIC-8 Tape and Reel Data FAIRCHILD SEMICONDUCTOR TM SOIC(8lds) Packaging Configuration: Figure 1.0 ATTENTION Packaging Description: Packaging Description: SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13° or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7° or 177cm diameter reel. This and some other options are further described in the Packaging Information table. Embossed ESD Marking Antistatic Cover Tape These full reside are individually barcode labeled and placed inside a standard intermediate box fillustrated in figure 10) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts. Static Dissipative **Embossed Carrier Tape** F63TNR Customized Label SOIC (8lds) Packaging Information L86Z **Packaging Option** F011 D84Z no flow code **SOIC-8 Unit Orientation** Packaging type TNR Qty per Reel/Tube/Bag 2,500 4,000 500 Reel Size 13" Dia 13" Dia 7" Dia Barcode Label Box Dimension (mm) 355x333x40 530x130x83 355x333x40 193x183x80 Max qty per Box 5.000 30.000 8.000 2.000 Weight per unit (gm) 0.0774 0.0774 0.0774 0.0774 Weight per Reel (kg) Barcode Label Barcode Label 355mm x 333mm x 40mm Intermediate container for 13" reel option F63TNR Label sample 193mm x 183mm x 80mm Pizza Box for Standard Option SOIC(8lds) Tape Leader and Trailer D/C1: Z9842AB QTY1: D/C2: QTY2: Configuration: Figure 2.0 (F63TNR)3 0 \bigcirc \bigcirc 0 \bigcirc \circ \bigcirc 0 0 0 0 0 0 Carrier Tape Components Cover Tape Leader Tape 1680mm minimum or 210 empty pockets Trailer Tape 640mm minimum or 80 empty pockets



SOIC(8lds) Embossed Carrier Tape



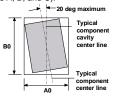


	Dimensions are in millimeter													
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	5.30 +/-0.10	6.50 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



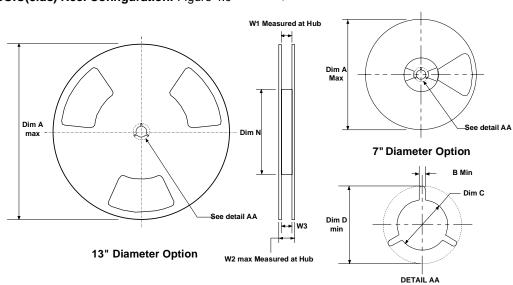
Sketch B (Top View)
Component Rotation



Sketch C (Top View)

Component lateral movement

SOIC(8lds) Reel Configuration: Figure 4.0

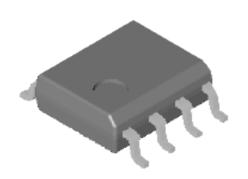


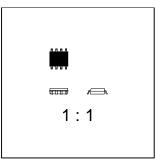
Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

SOIC-8 Package Dimensions



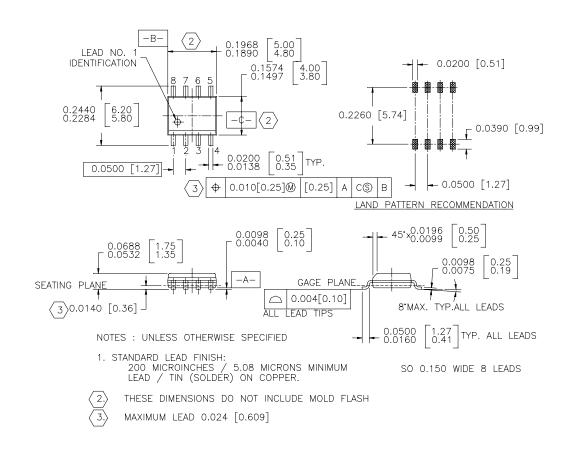
SOIC-8 (FS PKG Code S1)





Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

 $ACEx^{TM}$ FASTr™ PowerTrench® SyncFET™ Bottomless™ QFET™ TinyLogic™ GlobalOptoisolator™ QSTM UHC™ CoolFET™ GTO™ **VCX**TM $CROSSVOLT^{TM}$ QT Optoelectronics™ HiSeC™

DOME™ ISOPLANAR™ Quiet Series™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition				
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.				
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.				
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.				
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.				